

EAST - [jig.wsp:1]

File View Edit Tools Window Help

Drafts Pending Active

L1: (21245) flash and (memory or memories) and gate
L2: (944) 1 and (split adj gate)
L3: (909) 2 and ((control adj gate) or (floating adj gate))
L4: (444) 3 and spacer\$1
L5: (391) 4 and (control adj gate) and (floating adj gate)
L6: (389) 5 and ((source or drain) or (source adj drain))
L7: (378) 6 and gate.clm.
L8: (367) 7 and etch\$3
L9: (344) 8 and (mask or photoresist)
L10: (154) 9 and (select\$2 adj gate)
L11: (103) 10 and spacer\$1.clm.

DBs USPAF US-PGPUB Default Operator: OR Highlighted items only

11 and (select\$2 adj gate).clm.

Document ID Issue Date Pages Title Current CR Current Xref Retrieval C Inventor S C P I X

26	US 6096603 A	20000801	11	Method of fabricating a split gate structure of a fl	438/256	257/E21.638; 438/266		Chang, Kc-Hsing et al.	P F F F F F F F US
27	US 6005607 A	19991221	9	Method and apparatus for self-aligned memory cells an	365/185.26	257/E21.422; 257/E27.103;		Chen, Bin-Jhing	P F F F F F F F US
28	US 5989960 A	19991123	30	Semiconductor device and method for fabricating the s	438/267	257/E21.682; 257/E27.103;		Fukase, Kenji	P F F F F F F F US
29	US 5943261 A	19990624	16	Method for programming a flash memory	365/185.14	257/E21.422; 257/E29.129;		Lee, William W. Y.	P F F F F F F F US
30	US 5939749 A	19990817	23	Split gate transistor array	257/316	257/319; 257/900;		Taketa, Kaoru et al.	P F F F F F F F US
31	US 5796139 A	19980818	31	Semiconductor device	257/315	257/316; 257/E21.632;		Fukase, Kenji	P F F F F F F F US
32	US 5793079 A	19980811	21	Single transistor non-volatile electrically al	257/316	257/315; 257/320;		Georgescu, Sorin et al.	P F F F F F F F US
33	US 5702965 A	19971230	7	Flash memory cell and method of making the same	438/261	257/E21.422; 257/E29.129;		Kim, Jeoung Woo	P F F F F F F F US
34	US 5614747 A	19970325	13	Method for manufacturing a flash EEPROM cell	257/316	257/319; 257/321;		Ahn, Byung J. et al.	P F F F F F F F US
35	US 5554869 A	19960910	3	Electrically programmable read-only memory array	257/316	257/326; 257/903;		Chang, Kuo-Tung	P F F F F F F F US
36	US 5494838 A	19960227	10	Process of making EEPROM memory device having a sidew	438/264	257/E27.103; 257/E29.129;		Chang, Kuo-Tung et al.	P F F F F F F F US
37	US 5467308 A	19951114	11	Cross-point eeprom memory array	365/105.01	257/314; 257/316;		Chang, Kuo-Tung et al.	P F F F F F F F US
38	US 5455792 A	19951003	21	Flash EEPROM devices employing mid channel inject	365/185.15	257/316; 257/319;		Yi, Yong-Wan	P F F F F F F F US
39	US 5422504 A	19950606	12	EEPROM memory device having a sidewall spacer floating g	365/185.15	257/315; 257/321;		Chang, Kuo-Tung et al.	P F F F F F F F US
40	US 5408115 A	19950418	9	Self-aligned, split-gate EEPROM device	257/324	257/314; 257/326;		Chang, Kuo-Tung	P F F F F F F F US

Ready

NUM: